FIG. 6F

PLL SYSTEM
LEVEL EQUATIONS
600F

STABILITY

$$PLL.CROSS\_OVER\_FREQ = \frac{LF.R(PFD.GAIN)\,(CP.IP)\,(VCO.GAIN)}{DIV.M} \leftarrow 631$$

$$PLL.PHASE\_MARGIN = \Pi/2 - \frac{1}{PLL.CROSS\_OVER\_FREQ\,(LF.R)\,(LF.C2)} - PLL.CROSS\_OVER\_FREQ\,(LF.R)\,(LF.C2) \quad \Big\} 632$$

$$-PLL.CROSS\_OVER\_FREQ\,(VCD.TAU3)$$

$$PLL.CROSS\_OVER\_FREQ \leq PLL.CROSS\_OVER\_FREQ\_USER\_SPEC \leftarrow 633$$

$$PLL.PHASE\_MARGIN \geq PLL.PHASE\_MARGIN\_USER\_SPEC \leftarrow 634$$

635

PEAK
JITTER

$$PLL.PEAK\_JITTER = \frac{VCO.KAPPA\,(2\Pi)^{0.5}\,(DIV.M)^{0.5}\,(LF.C1)^{0.5}}{(PFD.GAIN)^{0.5}\,(CP.IP)^{0.5}\,(VCO.GAIN)^{0.5}} \leftarrow 635a$$

$$+ \frac{3(\sin[\Pi(SEC.TRESET)\,(PLL.INPUT\_REF\_SIGNAL\_FREQ)])\,(CP.DELTA\_IP)\,(VCO.GAIN)\,(LF.R)\overbrace{\propto(LF.R)\,(LF.C2)\,2\Pi\,(PLL.INPUT\_REF\_SIGNAL\_FREQ)B}^{635b1}}{\Pi^2\,(PLL.INPUT\_REF\_SIGNAL\_FREQ)\,(DIV.M)}$$

$$PLL.PEAK\_JITTER \leq PLL.PEAK\_JITTER\_USER\_SPEC \leftarrow 636$$

635b

POWER
SUPPLY
REJECTION

$$PLL.VDD\_DC = VCO.VDD\_DC \leftarrow 637$$

$$PLL.VDD\_DC \leq PLL.VDD\_DC\_USER\_SPEC \leftarrow 638$$

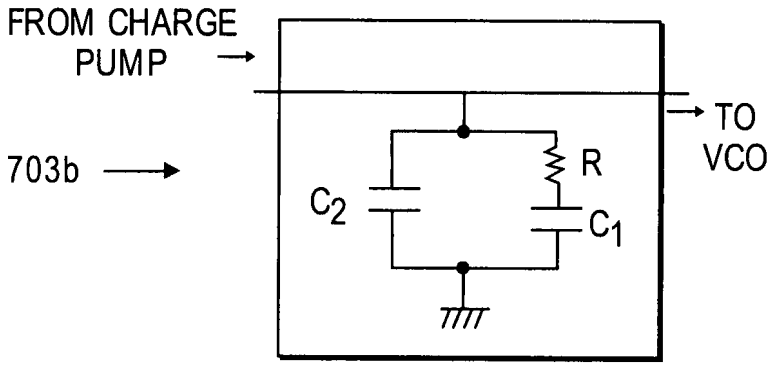

FIG. 7C

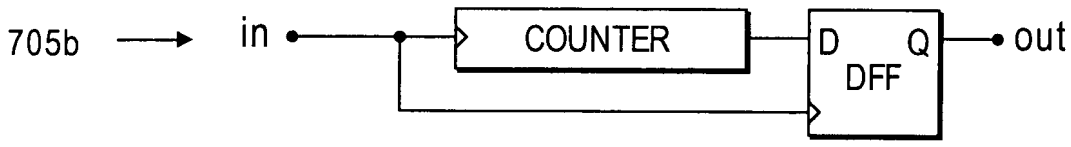

FIG. 7D